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Substitute for form 1449A/PTO		MAR 31 2004		Complete if Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				Application Number	09/891,523
				Filing Date	June 27, 2001
				First Named Inventor	Ryan N. RAKVIC et al.
				Art Unit	2188
				Examiner Name	Midys INOA
Sheet	1	of	2	Attorney Docket Number	02207/1123601

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
MI	1	4,905,141	02/27/1990	Brenza	
MI	2	5,381,533	01/10/1995	Peleg et al.	
MI	3	5,796,978	08/18/1998	Yoshioka et al.	
MI	4	6,128,704	10/03/2000	Jun	
MI	5	6,167,510	12/26/2000	Tran	
MI	6	6,327,643 B1	12/04/2001	Egan	
MI	7	6,349,364 B1	02/19/2002	Kai et al.	
MI	8	6,549,987 B1	04/15/2003	Rappoport et al.	
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FOREIGN PATENT DOCUMENTS						
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		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

Examiner Signature	Midys Inoa	Date Considered	9/3/04
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Substitute for form 1449B/PTO		<b>Complete if Known</b>			
		Application Number	09/891,523		
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		Filing Date	June 27, 2001		
		First Named Inventor	Ryan N. RAKVIC et al.		
		Art Unit	2188		
		Examiner Name	Midys INOA		
Sheet	2	of	2	Attorney Docket Number	02207/1123601

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
MI	9	BLACK et al, "The Block-Based Trace Cache", Proceedings of The 26th Int'l. Symposium on Computer Architecture, pp. 196-207, May 2-4, 1999, Atlanta, Georgia	
MI	10	CONTE et al, "Optimization of Instruction Fetch Mechanisms for High Issue Rates", Proceedings of the 22nd Annual Int'l Symposium on Computer Architecture, pp. 333-344, June 22-24, 1995, Santa Margherita Ligure, Italy	
MI	11	DUTTA et al, "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors", Proceedings of The 28th Int'l. Symposium on Microarchitecture, pp. 258-263, Nov. 29 - Dec. 1, 1995, Ann Arbor, Michigan	
MI	12	FRIENDLY et al, "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", Proceedings of The 30th Annual IEEE/ACM Int'l Symposium on Microarchitecture, pp. 24-33, Dec. 1-3, 1997, Research Triangle Park, North Carolina	
MI	13	INTRATER et al, "Performance Evaluation of a Decoded Instruction Cache for Variable Instruction-Length Computers", Proceedings of the 19th Annual Int'l Symposium on Computer Architecture, pp. 108-113, May 19-21, 1992, Gold Coast, Australia	
MI	14	JACOBSON et al, "Path-Based Next Trace Prediction", Proceedings of the 30th Annual Int'l Symposium on Microarchitecture, pp. 14-23, December 1-3, 1997, Research Triangle Park, North Carolina	
MI	15	MCFARLING, SCOTT, "Combining Branch Predictors", June, 1993, WRL Technical Note TN-36, Digital Western Research Laboratory, pp. i-25, Palo Alto, California	
MI	16	MICHAUD et al, "Exploring Instruction-Fetch Bandwidth Requirement in Wide-Issue Superscalar Processors", Proceedings of the 1999 Int'l Conference on Parallel Architectures and Compilation Techniques, pp. 2-10, October 12-16, 1999, Newport Beach, California	
MI	17	PATEL et al, "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing", Proceedings of The 25th Annual Int'l Symposium on Computer Architecture, pp. 262-271, June 27 - July 1, 1998, Barcelona, Spain	
MI	18	REINMAN et al, "A Scalable Front-End Architecture for Fast Instruction Delivery", Proceedings of the 26th Int'l Symposium on Computer Architecture, pp. 234-245, May 2-4, 1999, Atlanta, Georgia	
MI	19	ROTENBERG et al, "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings of the 29th Annual IEEE/ACM Int'l Symposium on Microarchitecture, MICRO-29, pp. 24-34, December 2-4, 1996, Paris, France	
MI	20	SEZNEC et al, "Multiple-Block Ahead Branch Predictors", Proceedings of the 7th Int'l Conference on Architectural Support for Programming Languages and Operating Systems, pp. 116-127, October 1-4, 1996, Cambridge, USA	
MI	21	YEH et al, "Increasing the Instruction Fetch Rate via Multiple Branch Prediction and A Branch Address Cache", Proceedings of the 7th Int'l Conference on Supercomputing, pp. 67-76, July 1993, Ann Arbor, Michigan	

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

## Complete If Known

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First Named Inventor RAKVIC et al  
Group Art Unit 2188  
Examiner Name M. Inoa  
Attorney Docket Number 2207/1123601

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## U.S. PATENT DOCUMENTS

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		Number	Kind Code <sup>2</sup> (if known)			
MI		5,495,617		Yamada	2/27/96	
MI		5,634,131		Matter et al	5/27/97	
MI		6,608,476	B1	Mirov et al	8/19/03	
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MI		6,427,188	B1	Lyon et al	7/30/02	
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MI		6,219,796	B1	Bartley	4/17/01	
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## FOREIGN PATENT DOCUMENTS

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		Office	Number <sup>4</sup>				
MI			WO 97/37307	Intel Corporation	10/9/97		

## OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

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